

**UNITED STATES PATENT APPLICATION**

**OF**

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**FOR**

**NARROW FINS BY OXIDATION  
IN DOUBLE-GATE FINFET**

NARROW FINS BY OXIDATION  
IN DOUBLE-GATE FINFET

TECHNICAL FIELD

[0001] The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).

BACKGROUND ART

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are, therefore, being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

[0005] Implementations consistent with the present invention provide an exemplary process for forming double fins for a double-gate FinFET. The exemplary process, consistent with the invention, improves short-channel effects in the FinFET by thinning the double fins to create

narrow fins using, for example, a thermal oxidation process. The exemplary double fin formation process may also, consistent with the invention, increase the device density, thus, reducing the pitch.

**[0006]** Additional advantages and other features of the invention will be set forth in part in the description which follows and, in part, will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

**[0007]** According to the present invention, the foregoing and other advantages are achieved in part by a method of forming fins for a double-gate fin field effect transistor (FinFET). The method includes forming a second layer of semi-conducting material over a first layer of semi-conducting material and forming double caps in the second layer of semi-conducting material. The method further includes forming spacers adjacent sides of each of the double caps and forming double fins in the first layer of semi-conducting material beneath the double caps. The method also includes thinning the double fins to produce narrow double fins.

**[0008]** According to another aspect of the invention, a method of forming fins for a double-gate fin field effect transistor (FinFET) is provided. The method includes depositing a silicon layer over a buried oxide layer and depositing a  $\text{Si}_3\text{N}_4$  layer over the silicon layer. The method further includes etching the  $\text{Si}_3\text{N}_4$  layer to form double caps, wherein each of the double caps comprises a rectangular cross-section with a width ranging from about 100 Å to about 1000 Å, and depositing and etching an oxide material to form spacers adjacent sides of each of the double caps, wherein the oxide material includes  $\text{SiO}$  or  $\text{SiO}_2$ . The method also includes etching the silicon layer to form fins beneath each of the double caps and thermally oxidating the fins to thin the fins so as to produce narrow fins, wherein each of the narrow fins has a thickness ranging from about 50 Å to about 500 Å.

**[0009]** Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0010]** Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

**[0011]** FIG. 1 illustrates exemplary layers of a silicon-on-insulator (SOI) wafer that may be used for forming a double-gate FinFET consistent with the present invention;

**[0012]** FIGS. 2A and 2B illustrate the formation of caps on the fin layer of FIG. 1 consistent with the invention;

**[0013]** FIG. 3 illustrates the formation of spacers adjacent the caps of FIGS. 2A and 2B consistent with the invention;

**[0014]** FIG. 4 illustrates the formation of double fins from the fin layer of FIG. 3 consistent with the invention;

**[0015]** FIGS. 5A and 5B illustrate thinning of the double fins of FIG. 4 consistent with the invention;

**[0016]** FIG. 6 illustrates the formation of a bottom gate layer, gate insulation layer and channel layer for a planar FinFET consistent with another embodiment of the invention;

**[0017]** FIG. 7 illustrates the formation of another gate insulation layer and a top gate layer on the channel layer of FIG. 6 consistent with another embodiment of the invention; and

**[0018]** FIGS. 8A and 8B illustrate the formation of a selected dielectric layer on a FinFET fin to

induce strain within the FinFET channel consistent with yet another embodiment of the invention.

#### BEST MODE FOR CARRYING OUT THE INVENTION

**[0019]** The following detailed description of the invention refers to the accompanying drawings.

The same reference numbers in different drawings may identify the same or similar elements.

Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims.

**[0020]** Consistent with the present invention, an exemplary process for forming double fins for a double-gate FinFET is provided. The exemplary process may employ thermal oxidation for thinning the double fins to create narrow fins, thereby improving device short-channel effects.

**[0021]** FIG. 1 illustrates a cross-section of a silicon on insulator (SOI) wafer 100 formed in accordance with an exemplary embodiment of the present invention. SOI wafer 100, consistent with the present invention, may include a buried oxide layer 110 formed on a substrate 115. A fin layer 105 may further be formed on buried oxide layer 110. The thickness of fin layer 105 may range, for example, from about 100 Å to about 1000 Å and the thickness of buried oxide layer 110 may range, for example, from about 1000Å to about 3000Å. Fin layer 105 and substrate 115 may include, for example, silicon, though other semiconducting materials, such as germanium, may be used. A layer 120 of material, such as, for example,  $\text{Si}_3\text{N}_4$ , may be formed on fin layer 105. Layer 120 may be deposited on fin layer 105 and may range, for example, from about 50 Å to about 500 Å in thickness.

**[0022]** As shown in FIGS. 2A and 2B, two caps 205 may be defined in layer 120. Caps 205 may be defined, for example, using conventional etching processes and may have a width  $w_1$  that ranges from about 50 Å to about 500 Å. Spacers 305 may then be formed on the sides of caps 205, as shown in FIG. 3. Spacers 305 may be thermally grown, or deposited and etched, on

the sides of caps 205 and may include, for example, an oxide material. The oxide material may include, for example, SiO or SiO<sub>2</sub>, though other oxide materials may be used.

**[0023]** Two fins 405 may be formed from fin layer 105, as shown in FIG. 4. Fins 405 may be formed beneath spacers 305 and caps 205 using, for example, conventional etching processes. Fins 405 may include a width  $w_2$  ranging from about 50 Å to about 500 Å. Thermal oxidation may then be performed and the oxide removed to thin down fins 405 to create thinned fins 505, as shown in FIGS. 5A and 5B. The thickness  $t$  of thinned fins 505 may range from about 100 Å to about 1000 Å. Oxide spacers 305 may also be removed, as further shown in FIGS. 5A and 5B, during the oxide removal. The thinning of fins 505, thereby, improves the short-channel effects in a double-gate FinFET that can result from the above-described process (with the addition of double gates that are not shown). The exemplary process described above for forming thinned fins for a double-gate FinFET additionally may increase the device density, thus, reducing the device pitch.

#### EXEMPLARY METAL-INDUCED CRYSTALLIZATION FOR TOP-BOTTOM GATE DOUBLE GATE FINFET

**[0024]** FIGS. 6-7 illustrate an exemplary process for forming a planar double-gate FinFET with top/bottom gates using metal-induced crystallization. As shown in FIG. 6, a layer 610 of oxide, for example, may be grown on a bulk wafer that includes a substrate 605. Oxide layer 610 may include, for example, SiO or SiO<sub>2</sub>, though other oxide materials may be used, and may range, for example, from about 100 Å to about 500 Å in thickness. A layer 615 of material for a bottom gate may then be deposited on oxide layer 610. Layer 615 may include polysilicon or a metal material, such as, for example, TiN, W, or Mo, and may range from about 100 Å to about 500 Å in thickness. A gate insulation layer 620 may then be deposited on layer 615. Gate insulation layer 620 may include SiO, SiO<sub>2</sub>, SiN, SiON, HfO<sub>2</sub>, ZrO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfSiO(x), ZnS, MgF<sub>2</sub>, or other high-K dielectric materials. The thickness of gate insulation layer 620 may range, for example, from about 10 Å to about 50 Å. A channel layer 625 may then be deposited on gate insulation

layer 620. Channel layer 625 may include an amorphous silicon ( $\alpha$ -Si) material. Channel layer 625 may additionally include a layer of deposited nickel (Ni). After deposition of the nickel layer, the channel layer 625 may be annealed to convert the amorphous silicon and Ni to crystalline silicon via metal induced crystallization.

[0025] As shown in FIG. 7, a second gate insulation layer 630 may be deposited on channel layer 625. Gate insulation layer 630 may include SiO, SiO<sub>2</sub>, SiN, SiON, HfO<sub>2</sub>, ZrO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfSiO(x) ZnS, MgF<sub>2</sub>, or other high-K dielectric materials. The thickness of gate insulation layer 630 may range, for example, from about 10 Å to about 50 Å. A layer 635 of material for a top gate may then be deposited on oxide layer gate insulation layer 630. Layer 635 may include polysilicon or a metal material, such as, for example, TiN, W, or Mo, and may range from about 100 Å to about 500 Å in thickness. The layers of material for the bottom gate and top gate may then be etched (not shown) using conventional etching processes to provide appropriate definition for the gates. Subsequent to gate definition, the resulting FinFET includes a planar double-gate device with top and bottom gates that has a channel in between the top and bottom gates created using metal-induced crystallization.

#### EXEMPLARY GATE DIELECTRIC STRESSER

[0026] FIGS. 8A and 8B illustrate an exemplary FinFET gate dielectric, consistent with another embodiment of the invention, that improves FinFET carrier mobility. As shown, a fin 805 may be formed on a substrate 810, using any conventional technique, and a dielectric layer 815 may be thermally grown or deposited on the fin 805. The dielectric material of dielectric layer 815 may be chosen such that a desirable stress condition (i.e., due to tensile strain) may be created in fin 805, which represents the channel region of the FinFET. The dielectric material, such as a high dielectric constant dielectric material, may be appropriately selected to create tensile strain in the material that comprises fin 805. The induced tensile strain improves carrier mobility of the channel region, thus, improving FinFET performance.

[0027] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional photolithographic, etching and deposition techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0028] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.